Claims

What is claimed is:

1. A hybride prediction method usable in parallel computing processors comprising using strides for a last-value-prediction, for a stride-based value prediction and for a history-pattern-based value prediction.

2. The method according to claim 1, further comprising calculating a current stride from a compare between the last result value from an earlier completed instance of an instruction and the same instruction's current result, updating at least one counter of a plurality of saturating counters in a stride history tracking table according to the current stride, and predicting a value calculated from a compare of the last result value from an earlier completed instruction and the stride stored in a stride field containing a value beyond a hit threshold-value.

3. The method according to claim 1, further comprising for an instruction not yet stored in said first table, initializing a counter reflecting its current result value with one saturation value, and the remaining counters with the respective opposite saturation value, and updating the counters corresponding to the occurrence of values calculated from the completion of later instances of the same instruction.

4. The method according to claim 1, further comprising incrementing the respective counter on occurrence of the same stride as selectable by said counter, and decrementing the remaining counters, and predicting a value calculated from the stride selectable by the highest counter if the highest counter has a value above a predetermined threshold value.

5. The method according to claim 1, further comprising signalling that a value cannot be predicted when no counter is above said threshold value.

6. A hybride prediction system comprising circuits corresponding to a first table having a first plurality of entries, each entry comprising a second plurality of stride fields, a stride history pattern field, and a pattern history table storing the same second plurality of counters and being arranged to be addressable by a two-table look-up mechanism using a stride history pattern (SHP) for selecting an entry in said second table, and the counters being arranged for being updated according to the occurrences of repeated strides or stride patterns.

7. The hybride prediction system according to claim 6 in which the number of stride fields is greater than 3 and less than 7.

8. A sub-unit for use in microprocessor devices having at least one prediction system according to claim 7.

9. A microprocessor device having at least one sub-unit according to claim 8.

10. A computer system having a microprocessor device according to claim 9.

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